Amendments to the Claims

Claim 1 (withdrawn): A test configuration, comprising:

a semiconductor wafer;

a plurality of semiconductor chips disposed on said semiconductor wafer, each of said plurality of semiconductor chips having a self-test unit generating test information for functionally checking said semiconductor chip; and

an energy source disposed on said semiconductor wafer and connected to said semiconductor chip for providing an electrical energy supply to said semiconductor chip, said energy source having at least one solar cell for generating an operating current for said semiconductor chip by optical radiation fed in contactlessly, said solar cell being disposed on a surface of said semiconductor wafer remote from said semiconductor chip;

said semiconductor wafer having an electrically conductive plated-through hole formed therein disposed between said solar cell and said semiconductor chip, at a boundary between said plated-through hole and said semiconductor wafer, and said semiconductor wafer having a pn junction disposed along said plated-through hole for preventing a current flow between said

plated-through hole and a remainder of said semiconductor wafer.

Claims 2-6 (cancelled.)

Claim 7 (previously amended): The test configuration according to claim 20, including a radiation-absorbing layer disposed between said solar cell and said semiconductor chip.

Claim 8 (withdrawn): The test configuration according to claim 1, wherein said semiconductor chip has a functional unit for a contactless transmission of data containing information about a test result.

Claim 9 (withdrawn): The test configuration according to claim 8, including a receiver, and said functional unit generates optical radiation pulses in accordance with the data to be transmitted, which can be received by said receiver disposed separate from said semiconductor chip.

Claim 10 (withdrawn): The test configuration according to claim 8, including a receiver disposed separate from said semiconductor chip, said functional unit has an output terminal through which the data to be transmitted can be transmitted by capacitive coupling to said receiver.

Claim 11 (withdrawn): The test configuration according to claim 10, wherein said semiconductor chip has a material layer connected to said output terminal of said functional unit, at which a potential, which can be controlled by said functional unit, is present in accordance with the data to be transmitted, said material layer effects an optical refraction of optical radiation and the optical refraction can be controlled by the potential, said material layer can be irradiated with the optical radiation and the optical radiation refracted by said material layer can be received by said receiver.

Claim 12 (withdrawn): The test configuration according to claim 8, wherein said semiconductor chip has a detector selected from the group consisting of voltage detectors and current detectors, said detector is connected to said energy source and to said functional unit for initiating a data transmission by said functional unit on account of a detected characteristic voltage sequence or current sequence.

Claim 13 (withdrawn): The test configuration according to claim 1, wherein said semiconductor chip has a terminal and a nonvolatile memory unit for storing data containing information about a test result, said nonvolatile memory unit is connected to said terminal through which the data of said

nonvolatile memory unit can be tapped off to a point outside said semiconductor chip.

Claim 14 (withdrawn): The test configuration according to claim 1, wherein said semiconductor chip is one of a plurality of semiconductor chips to be tested, and one of said plurality of semiconductor chips to be tested is decoupled from respective others of said plurality of semiconductor chips with regard to said energy supply during a functional test.

Claim 15 (withdrawn): The test configuration according to claim 1, wherein said semiconductor chip is one of a plurality of semiconductor chips to be tested and all connected to said energy source being a common energy source, each of said semiconductor chips have a current limiter circuit for electrically isolating a respective semiconductor chip from said common energy source in an event of a limit value of an operating current being exceeded.

Claim 16 (withdrawn): The test configuration according to claim 1, wherein said semiconductor chip has a detector selected from the group consisting of voltage detectors and current detectors, said detector connected to said energy source and to said self-test unit for initiating a functional test on account of a detected characteristic voltage sequence or current sequence.

Claim 17 (withdrawn): The test configuration according to claim 1, wherein said semiconductor chip has an integrated memory containing memory cells which can be subjected to a functional test, and said self-test unit generates test information and carries out a functional test of said memory cells.

Claim 18 (withdrawn): The test configuration according to claim 17, wherein said integrated memory has normal memory cells and redundant memory cells for replacing said normal memory cells, said self-test unit is configured for checking a functionality of said normal memory cells, for analyzing which of said normal memory cells are to be replaced by which of said redundant memory cells, and for activating said redundant memory cells in accordance with a result of the analysis.

Claim 19 (withdrawn): The test configuration according to claim 18, wherein said integrated memory has electrically programmable memory units for activating said redundant memory cells, in which a repair result determined by said self-test unit can be programmed.

Claim 20 (currently amended): A test configuration, comprising:

a semiconductor wafer having a surface with an area;

a plurality of semiconductor chips disposed on said surface of said semiconductor wafer, each of said semiconductor chips having a self-test unit generating test information for functionally checking said semiconductor chip; and

an energy source disposed above said semiconductor wafer and connected to said semiconductor chip for providing an electrical energy supply to said semiconductor chip, said energy source having at least one solar cell for generating an operating current for said semiconductor chip by optical radiation fed in contactlessly, said solar cell being disposed areally ~~entirely~~ over said ~~area of said surface of said semiconductor wafer~~ semiconductor chips.

Claim 21 (previously added): The test configuration according to claim 20, including a radiation-absorbing layer between said solar cell and said semiconductor wafer, said radiation-absorbing layer having an electrically conductive plated-through hole formed therein disposed between said solar cell and said semiconductor chip.

Claim 22 (previously added): The test configuration according to claim 21, wherein said radiation-absorbing layer has a pn junction disposed along said plated-through hole at a boundary

between said plated-through hole and said radiation-absorbing layer for preventing a current flow between said plated-through hole and a remainder of said radiation-absorbing layer.

Claim 23 (previously added): The test configuration according to claim 20, wherein said semiconductor chip has a functional unit for a contactless transmission of data containing information about a test result.

Claim 24 (previously added): The test configuration according to claim 23, including a receiver disposed separate from said semiconductor chip, said functional unit having an output terminal through which the data to be transmitted can be transmitted by capacitive coupling to said receiver.

Claim 25 (previously added): The test configuration according to claim 23, wherein said semiconductor chip has a detector selected from the group consisting of voltage detectors and current detectors, said detector is connected to said energy source and to said functional unit for initiating a data transmission by said functional unit due to a detected characteristic voltage sequence or current sequence.

Claim 26 (previously added): The test configuration according to claim 20, wherein said semiconductor chip has a terminal

and a nonvolatile memory unit for storing data containing information about a test result, said nonvolatile memory unit being connected to said terminal through which the data of said nonvolatile memory unit can be tapped off to a point outside said semiconductor chip.

Claim 27 (previously added): The test configuration according to claim 20, wherein one of said semiconductor chips is decoupled from respective others of said semiconductor chips with regard to said energy supply during a functional test.

Claim 28 (previously added): The test configuration according to claim 20, wherein all of said semiconductor chips to be tested are connected to said energy source being a common energy source, each of said semiconductor chips has a current limiter circuit for electrically isolating a respective semiconductor chip from said common energy source in an event of a limit value of an operating current being exceeded.

Claim 29 (previously added): The test configuration according to claim 20, wherein each of said semiconductor chips has an integrated memory containing memory cells to be subjected to a functional test, and said self-test unit generates test information and carries out a functional test of said memory cells.

Claim 30 (previously added): The test configuration according to claim 29, wherein said integrated memory has normal memory cells and redundant memory cells for replacing said normal memory cells, and said self-test unit is configured for checking a functionality of said normal memory cells, for analyzing which of said normal memory cells are to be replaced by which of said redundant memory cells, and for activating said redundant memory cells in accordance with a result of the analysis.

Claim 31 (previously added): The test configuration according to claim 30, wherein said integrated memory has electrically programmable memory units for activating said redundant memory cells, in which a repair result determined by said self-test unit can be programmed.